Verification of Chiplet-based designs: Challenges and Solutions

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About me and Why I am here?

- I have deep expertise on verification of peripheral interconnects using Pure simulation and Emulation. Includes several broad market and turnkey projects from Unit Level to a complete System level testbench verification

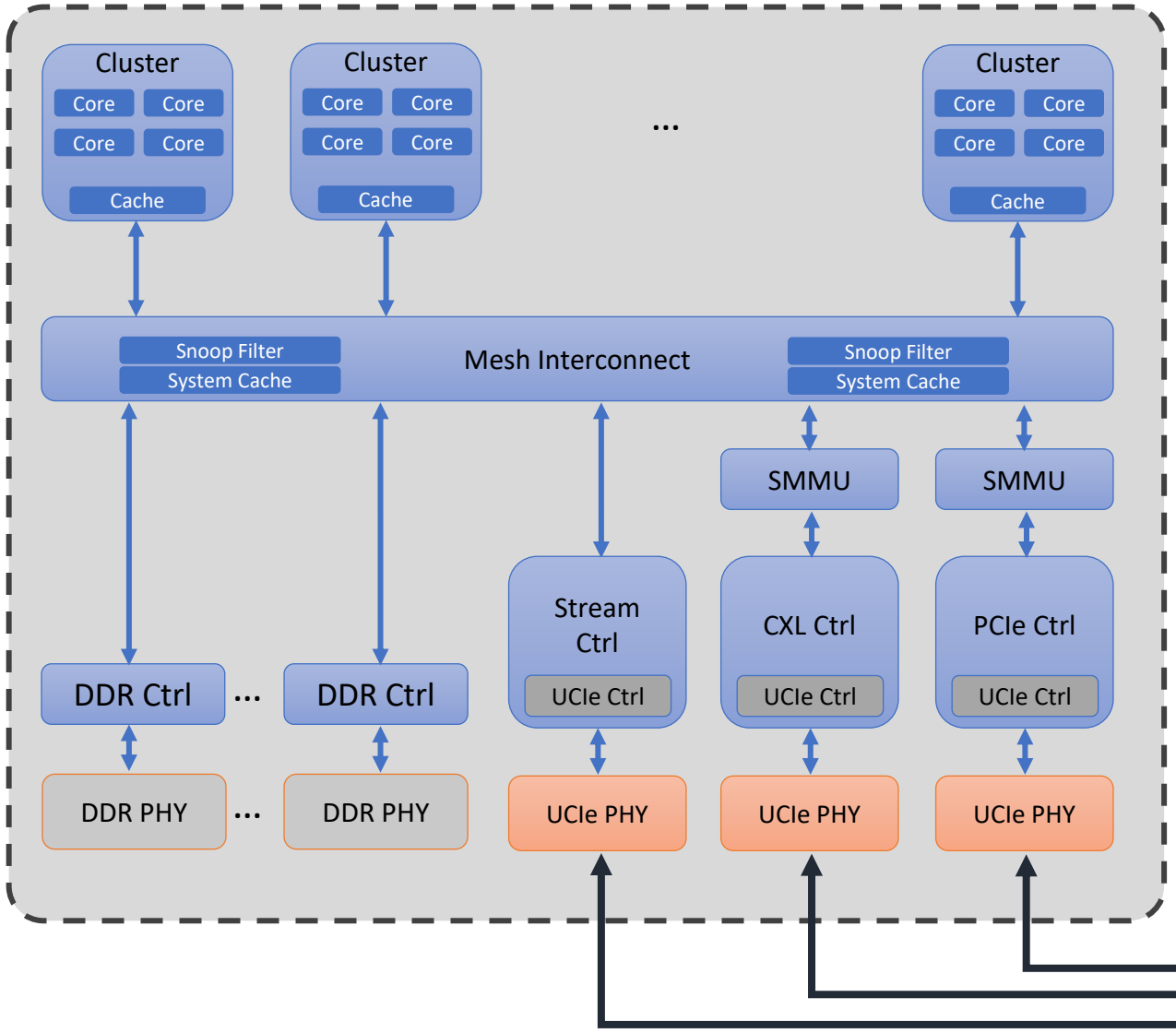
  At Cadence, I am responsible for defining models and methodologies for UCIe Verification by working with internal and external stakeholders

What to expect in this talk?

Leverage a simplified Dual Die Design as an Example and discuss state of the art techniques to address

- Individual Die Verification challenges
- System Level Coherency and Traffic Latency Analysis

UCIe in Action -Example Chiplet Design



- Explosion of Design Topologies
  - Several Unit Levels in different combinations
- Multiprotocol Verification
  - PCI Express using UCIe as the Transport Layer
  - CXL using UCIe as the Transport Layer
  - Streaming interface
- System Level Implications
  - -End-to-end Data Integrity
  - -Latency Calculation or Turn Around Time (TAT)

and more…

Companion Die

- Storage (CXL)
- High Speed I/O (PCIe)
- Symmetric Multi-Processor (Streaming)

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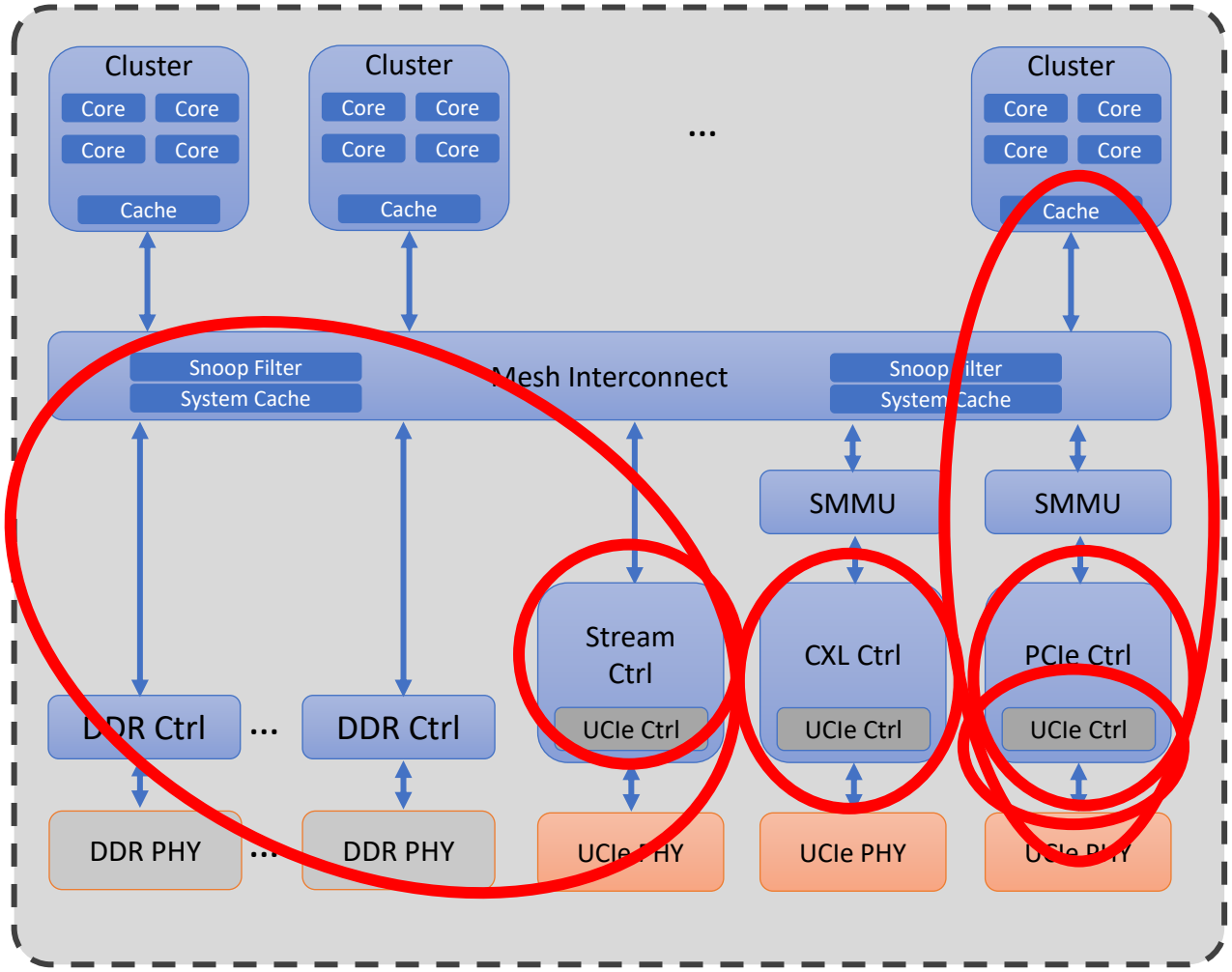
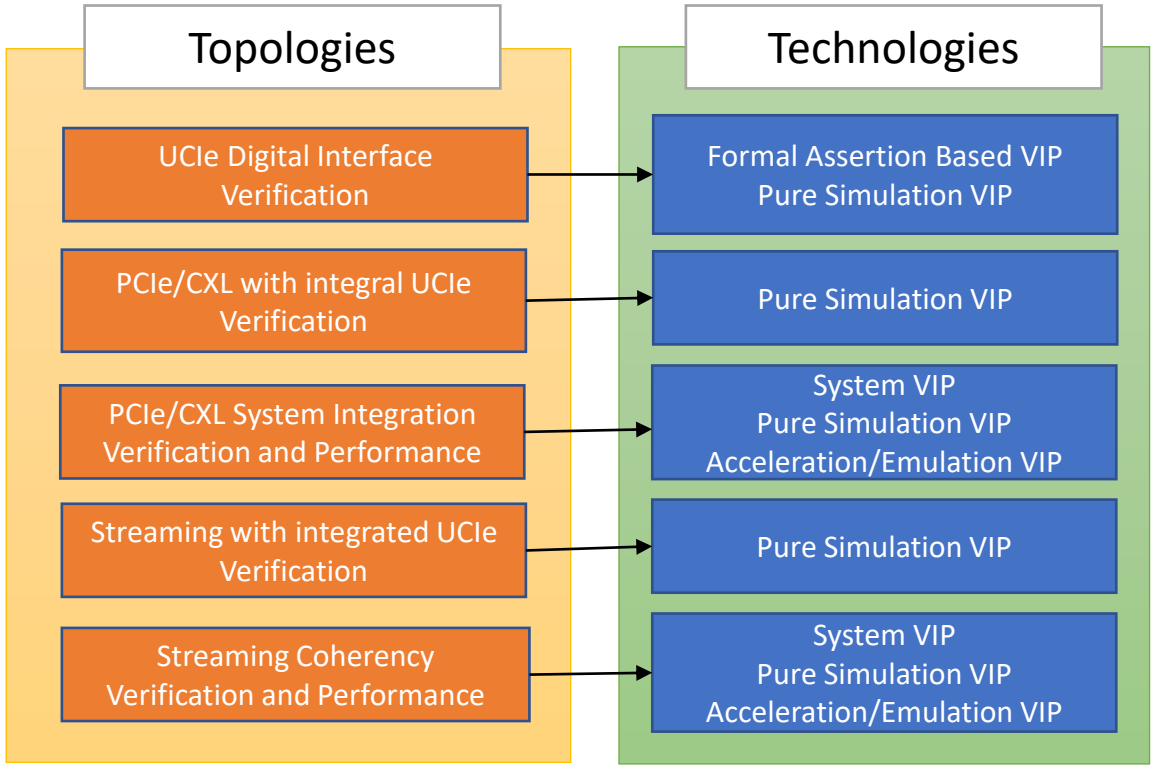
Verification Areas – Leverage Multiple Technologies





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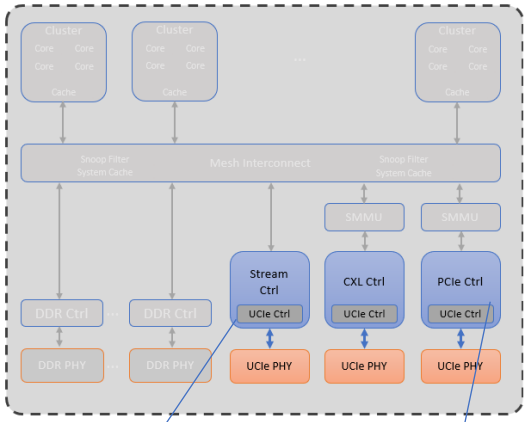
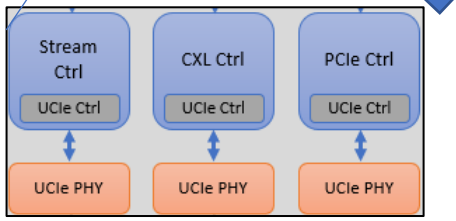
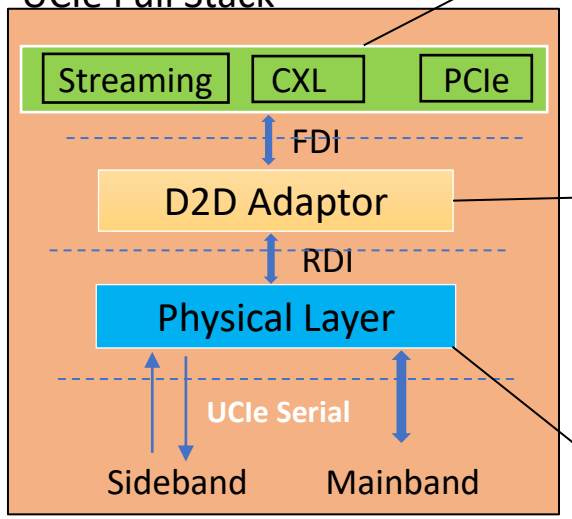
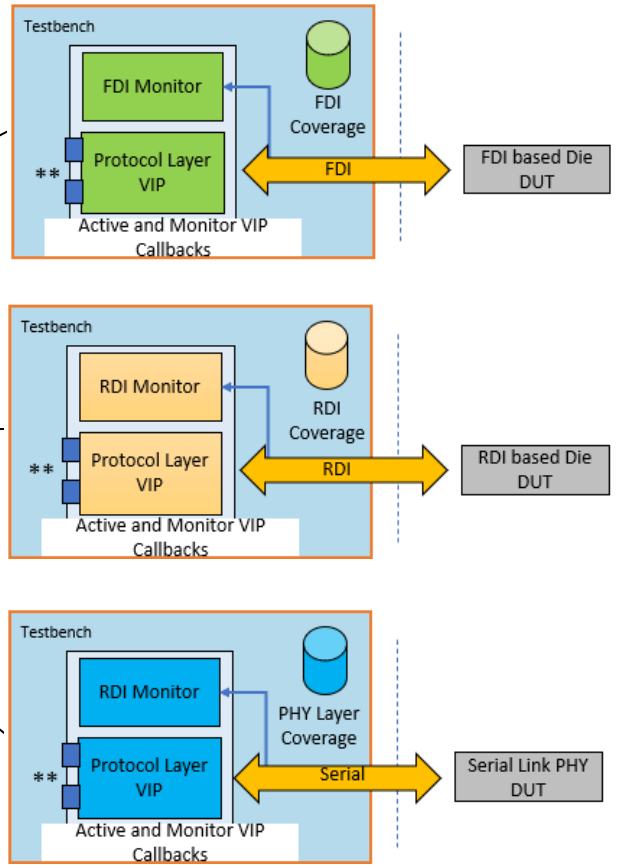
Solution - Die Disaggregated Verification









Verification Focus

- Die-to-Die Detailed protocol verification
- Observability & Controllability
- Full Callback & Error Injection
- Layer-wise scoreboard
- Interface-wise Coverage

Advantages

- No need for the entire design - Head start with verification prior to complete Design availability
- Expedite verification with Block level test cases
- IP design agnostic – Forward compatible
- Plug and Play at Subsystem/System level
- Bypass Link Training & Setup controls
- Bypass Interface dependency using Pseudo Ports

Key Takeaway

- LEGO-like detachable components configured as independent Chiplet interconnects of UCIe

**** Pseudo Ports are special Queues for Packet/Flit handling**

Legend

UCIe VIP/AVIP

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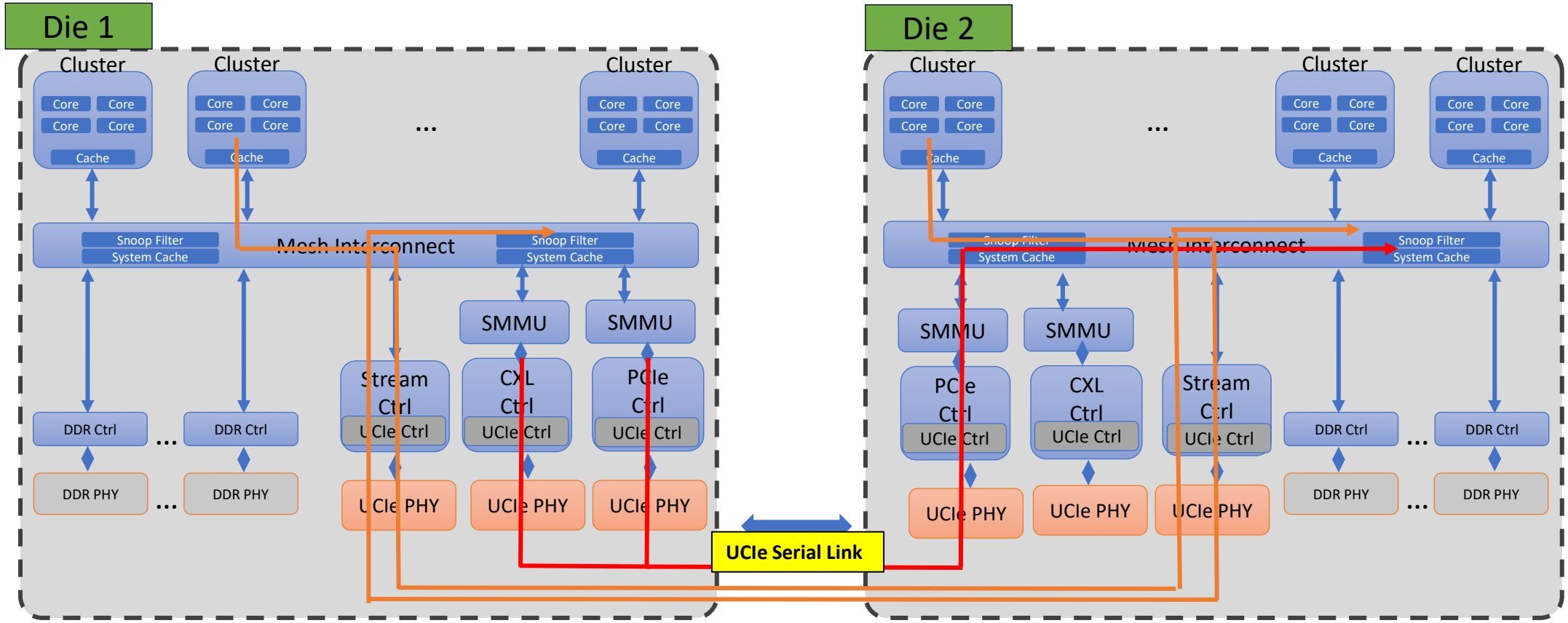
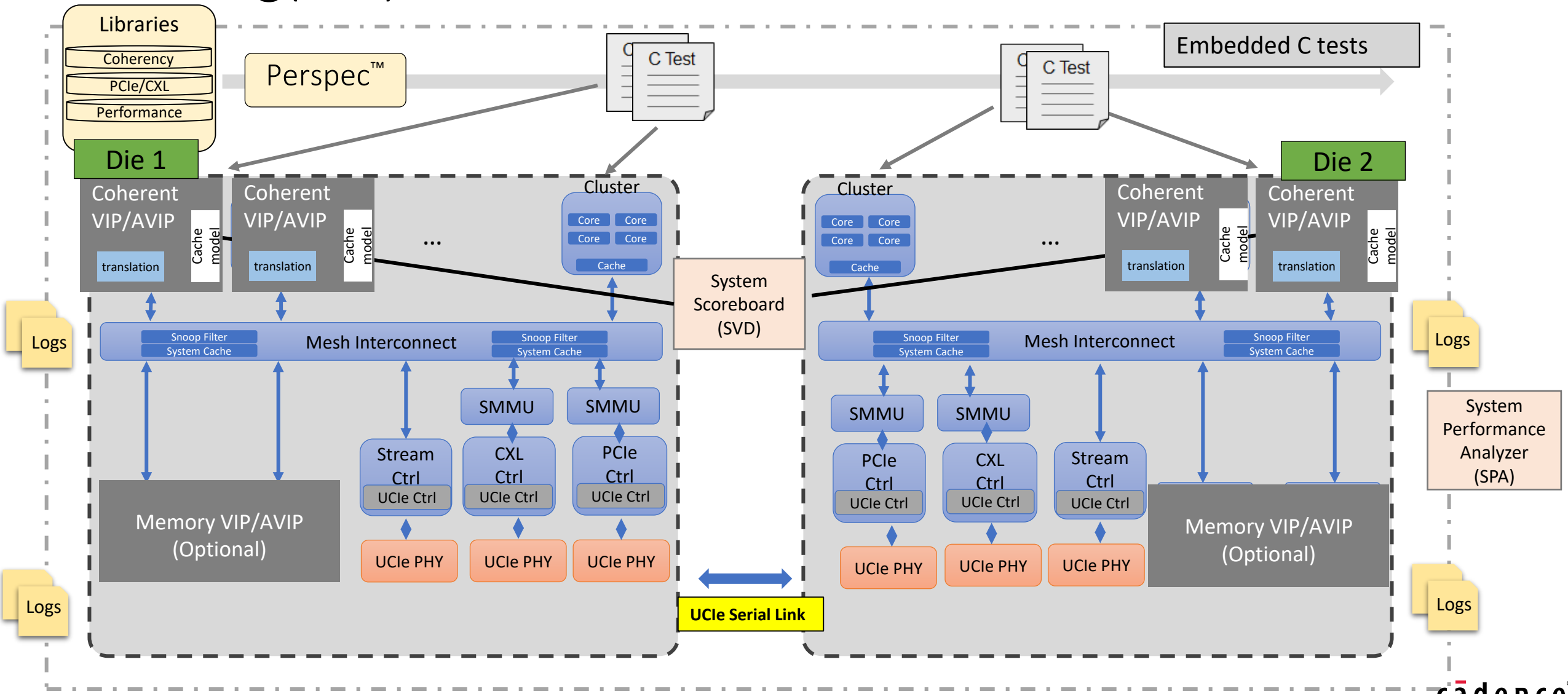
System Level- Performance Concerns

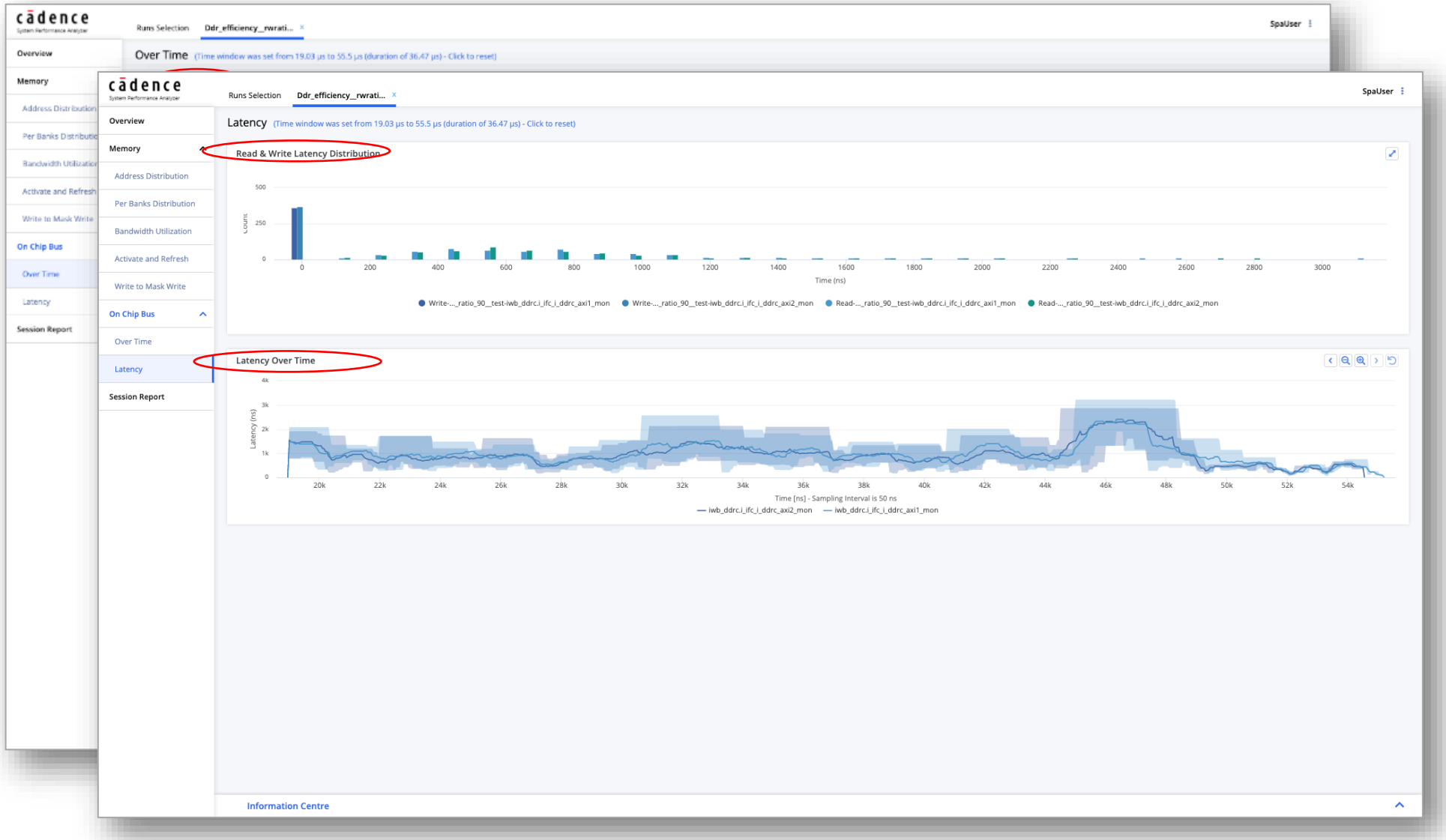


- Many steps in path from initiator to target, there are many potential ”throttle” points
- Understanding and debugging bandwidth throttling requires visualization of “throttle” proxies
  -Outstanding Transaction (OT) count is the standard measure
- Localization of cache lines can have a huge impact on latency and reduce die-to-die traffic (which itself can be a throttle)
- Data packet assembly and decomposition across the Chiplet Interconnects can add significant overhead

Solution- Complete System Performance & Integrity Checking(1/2)



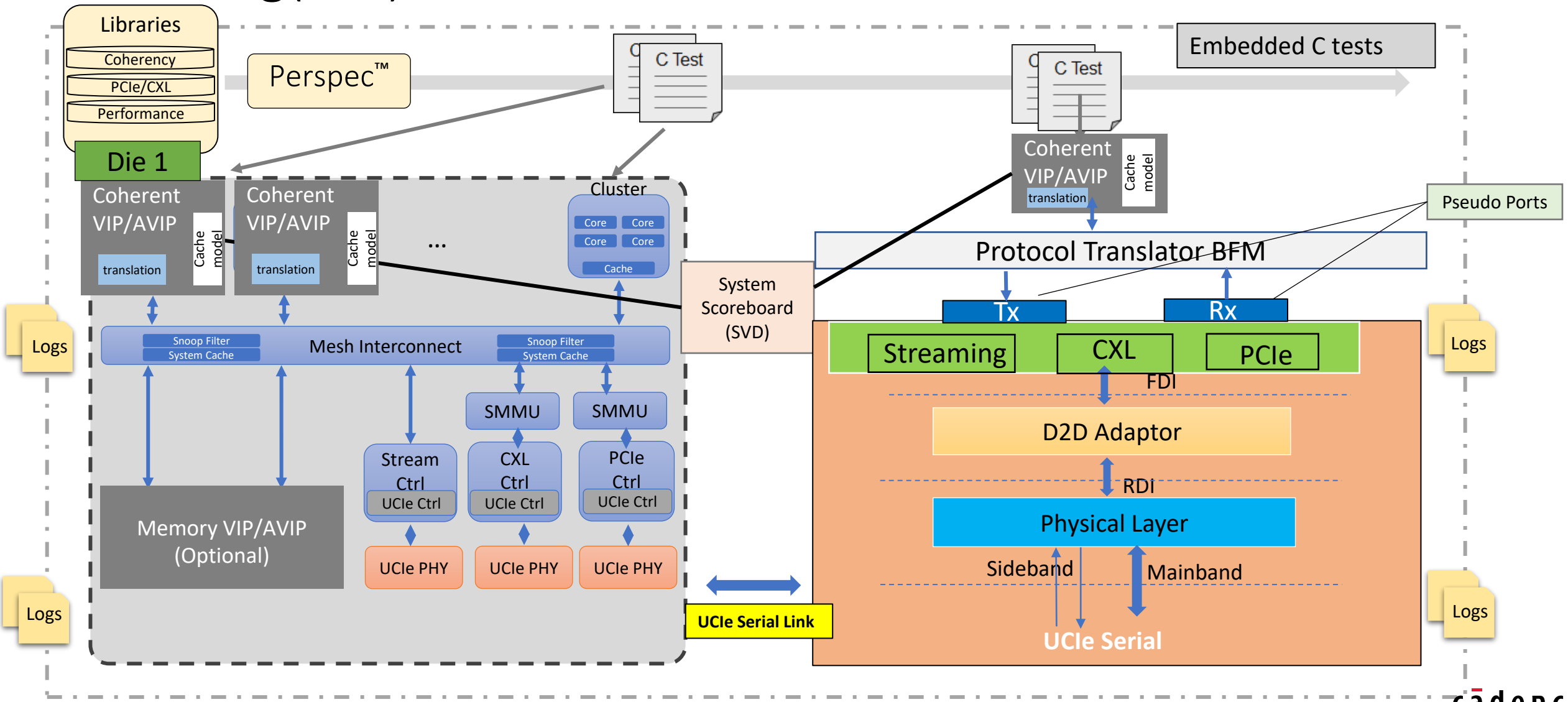
Screenshot-System Performance Analyzer(SPA)



Advantages

- Quickly understand the relationship between:
  - Bandwidth Over Time
  - Latency Over Time
  - Outstanding Transaction Over Time
- Allows bottlenecks to be identified and investigated
- Quickly identify outlier transactions with high latency and investigate the time period of occurrence

Solution- Complete System Performance & Integrity Checking(2/2)



Conclusion

- Individual Chiplet Interconnects need

  - Unit level detailed verification strategy

  - Early verification before full design availability

  - Scalable verification components to Subsystem/System level

- Multi Die System Verification needs

  - Deep Performance Analysis to identify Bottlenecks, Latency and calculate actual Bandwidth

  - Die-to-Die Scoreboards for Transaction Integrity

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